

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A method of calibrating a voltage controlled oscillator, comprising:

comparing a frequency of an output of a first voltage controlled oscillator to a reference frequency;

accumulating a first digital value relating to a difference in frequency between said output of said first voltage controlled oscillator and said reference frequency; and

controlling a frequency of said output of said first voltage controlled oscillator based on said accumulated first digital value;

comparing a frequency of an output of a second voltage controlled oscillator to said reference frequency;

accumulating a second digital value relating to a difference in frequency between said output of said second voltage controlled oscillator and said reference frequency; and

controlling a frequency of said output of said second voltage controlled oscillator based on said accumulated second digital value.

2. (original) The method of calibrating a voltage controlled oscillator according to claim 1, further comprising:

converting said accumulated first digital value into a first analog signal for control of said first voltage controlled oscillator.

3. (currently amended) ~~A~~ The method of calibrating a voltage controlled oscillator according to claim [[1]], further comprising:

comparing a frequency of an output of a first voltage controlled oscillator to a reference frequency;

accumulating a first digital value relating to a difference in frequency between said output of said first voltage controlled oscillator and said reference frequency;

controlling a frequency of said output of said first voltage controlled oscillator based on said accumulated first digital value; and

scanning said accumulated first digital value into a built-in self test (BIST) path.

4. (canceled)

5. (currently amended) The method of calibrating a voltage controlled oscillator according to claim 1 ~~[[4]]~~, further comprising:

comparing a frequency of an output of a third voltage controlled oscillator to said reference frequency;

accumulating a third digital value relating to a difference in frequency between said output of said third voltage controlled oscillator and said reference frequency; and

controlling a frequency of said output of said third voltage controlled oscillator based on said accumulated third digital value.

6. (original) The method of calibrating a voltage controlled oscillator according to claim 5, further comprising:

comparing a frequency of an output of a fourth voltage controlled oscillator to said reference frequency;

accumulating a fourth digital value relating to a difference in frequency between said output of said fourth voltage controlled oscillator and said reference frequency; and

controlling a frequency of said output of said fourth voltage controlled oscillator based on said accumulated fourth digital value.

7. (original) The method of calibrating a voltage controlled oscillator according to claim 6, further comprising:

scanning each of said first digital value, said second digital value, said third digital value, and said fourth digital value into a built-in self test (BIST) path.

8. (original) A method of calibrating a voltage controlled oscillator in a clock and data recovery (CDR) circuit, comprising:

selecting a calibration mode for at least one voltage controlled oscillator in said CDR circuit, while another voltage controlled oscillator is in an operational mode;

comparing a frequency of an output of said at least one voltage controlled oscillator to a reference frequency;

accumulating a digital value relating to a difference in frequency between said output of said at least one voltage controlled oscillator and said reference frequency; and

controlling a frequency of said output of said at least one voltage controlled oscillator based on said accumulated digital value.

9. (original) The method of calibrating a voltage controlled oscillator in a clock and data recovery (CDR) circuit according to claim 8, further comprising:

converting said accumulated digital value into an analog signal for control of said at least one voltage controlled oscillator.

10. (original) The method of calibrating a voltage controlled oscillator in a clock and data recovery (CDR) circuit according to claim 8, further comprising:

scanning said accumulated digital value into a built-in self test (BIST) path.

11. (currently amended) A clock and data recovery circuit, comprising:

a plurality of voltage controlled oscillators, each adapted for synchronization with a received data stream;

a state machine to select a calibration mode for any of said plurality of voltage controlled oscillators;

a frequency locked calibration loop to compare a frequency output from any of said plurality of voltage controlled oscillators to a reference frequency; and

an accumulator receiving an output from said frequency locked loop, an output of which controls a frequency output from any one of said plurality of voltage controlled oscillators to within a desired tolerance of said reference frequency.

12. (original) The clock and data recovery circuit according to claim 11, further comprising:

a data sampler adapted to extract data from said received data stream.

13. (original) The clock and data recovery circuit according to claim 11, wherein:

said accumulator is a digital accumulator.

14. (original) The clock and data recovery circuit according to claim 13, further comprising:

a digital-to-analog converter (DAC) to convert an output of said digital accumulator into an analog frequency control signal for control of a given one of said plurality of voltage controlled oscillators.

15. (original) The clock and data recovery circuit according to claim 13, further comprising:

a plurality of digital-to-analog converters (DACs) to convert an output of said digital accumulator into a respective analog frequency control signal for control of respective ones of said plurality of voltage controlled oscillators.

16. (currently amended) An integrated circuit including a clock and data recovery circuit, comprising:

a plurality of voltage controlled oscillators, each adapted for synchronization with a received data stream;

a state machine to select a calibration mode for any of said plurality of voltage controlled oscillators;

a frequency locked calibration loop to compare a frequency output from any of said plurality of voltage controlled oscillators to a reference frequency; and

an accumulator receiving an output from said frequency locked loop, an output of which controls a frequency output from any one of said plurality of voltage controlled oscillators to within a desired tolerance of said reference frequency.

17. (original) The integrated circuit including a clock and data recovery circuit according to claim 16, further comprising:

a data sampler adapted to extract data from said received data stream.

18. (original) The integrated circuit including a clock and data recovery circuit according to claim 16, wherein:

said accumulator is a digital accumulator.

19. (original) The integrated circuit including a clock and data recovery circuit according to claim 18, further comprising:

a digital-to-analog converter (DAC) to convert an output of said digital accumulator into an analog frequency control signal for control of a given one of said plurality of voltage controlled oscillators.

20. (original) The integrated circuit including a clock and data recovery circuit according to claim 18, further comprising:

a plurality of digital-to-analog converters (DACs) to convert an output of said digital accumulator into a respective analog frequency control signal for control of respective ones of said plurality of voltage controlled oscillators.